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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/747,703	12/21/2000	Thomas D. Nguyen	LAM1P155/P0700	9960

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EXAMINER
KORNAKOV, MICHAIL

ART UNIT	PAPER NUMBER
1746	4

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Please find below and/or attached an Office communication concerning this application or proceeding.

mk-4

Office Action Summary	Application No. 09/747,703	Applicant(s) NGUYEN, THOMAS D.	
	Examiner Michael Kornakov	Art Unit 1746	

-- The MAILING DATE of this communication appears on th cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *19 and 20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-20* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 December 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1-18, drawn to a method of processing a wafer, classified in class 134, subclass 6.

   II. Claims 19 and 20, drawn to a system for reducing He backside faults, classified in class 15, subclass 21.1+.

The inventions are distinct, each from the other because of the following reasons:

2. Inventions of Group I and Group II are related as process and apparatus for its practice. The inventions are distinct if it can be shown that either: (1) the process as claimed can be practiced by another materially different apparatus or by hand, or (2) the apparatus as claimed can be used to practice another and materially different process. (MPEP § 806.05(e)). In this case the process as claimed can be practiced in a single module apparatus, wherein the front or processing side of the substrate is protected and not effectuated by the process of back side cleaning.

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

4. Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

5. During a telephone conversation with Mr. Q. Hoellwarth on July 11, 2002 a provisional election was made without traverse to prosecute the invention of Group I, claims 1-18. Affirmation of this election must be made by applicant in replying to this Office action. Claims 19 and 20 withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Drawings

6. Figure 1A and 1B should be designated by a legend such as --Prior Art— because, as per Page 1, line 15 of the instant disclosure, they provide "a typical processing module" and, thus, only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

8. Claims 1, 4-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Prall et al. (U.S. 5,958,796).

Prall teaches a method of manufacturing a semiconductor device on a wafer, which has previously formed intermediate electronic components on the front side (compare to process side, as instantly claimed) and accumulation of waste matter (compare to un-wanted particles, as instantly claimed) on the backside. The method of Prall comprises depositing a cover layer over the front side, removing the waste matter from the back side of the wafer to provide a clean surface on the back side of the wafer and fabricating components on the front side of the wafer by performing etching or deposition on the front side of the wafer (see Abstract; col. 7, lines 31-67; col.4, lines 1-45). The waste matter from the back side of the wafer is removed by planarizing, utilizing polyurethane matrix material and chemicals, which removes any scratches and produces a **uniformly planar** polished surface (paragraph, bridging col.4 and 5; col.5, lines 48-53). Because Prall indicates subsequent processing of his wafers in a normal step in the process for etching vias and depositing conductive material on top of the insulating material and into the vias (col.8, lines 35-45), the step of transferring the wafer to the processing module is inherent

Therefore, all the limitations of instant claims either explicitly or inherently disclosed by Prall.

9. Claims 1 and 4-10 are rejected under 35 U.S.C. 102(b) as being anticipated by La et al. (U.S. 6,136,510).

La teaches a method of manufacturing a semiconductor device, which comprises the steps of providing a wafer having a frontside and a backside and scrubbing the backside of the wafer prior to performing the photolithographic technique to remove particulate contaminants from the wafer backside (col.2, lines 10-14, lines 26-35). Backside scrubbing is effected by processing **only the backside** of the wafer by a scrubbing operation employing a brush, preferably made of a synthetic plastic, e.g. PVA. (col.4, lines 1-6) and 1% solution of NH_4OH (col.6, line 16). The processing, subsequent to scrubbing the backside of the wafer, comprises etching through the photoresist mask to form a through hole, wherein plasma or reactive ion etching is utilized (col.5, lines 21-28; col.7, lines 31-37). Thus, the step of transferring wafer from scrubbing apparatus to the processing module is inherent.

Therefore, all the limitations of instant claims either explicitly or inherently disclosed by La.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

12. Claims 2, 3, 11, 12, 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Prall et al. (U.S. 5,958,796) in view of Guo et al. (U.S. 6,251,759).

While disclosing the steps of further etching or deposition on the front side of the wafer, Prall remains silent about placing wafer on a chuck. However, a chuck is a conventional element of deposition or etching apparatus, which allows to fix a wafer during processing and, therefore, a step of placing a wafer on the chuck is conventional in semiconductor processing, as evidenced, for example, by Guo (col. Fig.2; col. 5, line 66; col.6, lines 11-13). Thus, the skilled artisan would have found it obvious to place a wafer of Prall on the chuck, as advised by Guo in order to properly retain the wafer during the deposition or etching procedures of Prall.

While cleaning the back side of the wafer, Prall does not specifically emphasizes the issue of preventing gaps between the backside of the wafer and a chucking surface. However, Prall indicates that the waste matter from the back side of the wafer is removed by planarizing, using polyurethane matrix material and chemicals, which removes any scratches and produces a **uniformly planar** polished surface, thus eliminating any contact discrepancy between the wafer and its supporting surface, such as chucking surface, utilized during the further processing.

With regard to claims 11, 12, 14-18 Guo provides a cluster apparatus, which comprises load locks (col. 4, line 5), orientation chambers (col. 4, line 6) (compare to

aligner, as instantly claimed), preclean chambers (col.4, lines 7), robotic transport mechanism (col.4, line 35) and process chambers. Guo indicates that in a typical process sequence the wafer is oriented (compare to "aligned", as instantly claimed), moved into preclean chamber for cleaning and then into CVD or PVD plasma chamber (col. 4, lines 40-55; col.6, lines 6-12; Fig1).

Because Prall teaches deposition process on the front side of the wafer after removing the unwanted matter from its back side, however remains silent about particularities of his process and Guo teaches method and apparatus for depositing material upon a semiconductor wafer utilizing cluster tool and provides for precleaning of the wafer, one skilled in the art would have found it obvious to utilize the processing steps, performed in cluster apparatus of Guo, in the teaching of Prall in order to eliminate unnecessary exposure of processing wafer to environment, thus avoiding contamination, provide better control of the fabrication process and improve it output.

With regard to specific order of performing steps, as per claims 16-18, first of all, the sequence of steps is not specifically elucidated in the above claims, and secondly, selection of any order of performing steps is prima facie obvious in the absence of a new and unexpected results. Consult In re Burnhans, 154F.2d690, 69 USPQ 330 (CCPA 1946) and consult also Ex parte Rubin, 128 USPQ 440 (Bd.App.1959).

13. Claims 2, 3, 11, 13, 14 and 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over La et al. (U.S. 6,136,510) in view of Loan et al. (U.S. 6,136,725).

The teaching of La remains silent about the steps of placing wafer on the chuck while performing the processing task and preventing gaps between the backside of the wafer and a chucking surface. La also does not specifically indicates providing a heat transfer system inside the chuck. However, as indicated above, a chuck is a conventional element of deposition or etching apparatus, which supports and keeps wafer in place during processing, therefore, a step of placing a wafer on the chuck is conventional in semiconductor processing, as evidenced, for example, by Loan (paragraph, bridging col. 8 and 9). Thus, the skilled artisan would have found it obvious to place a wafer of La on the chuck, as advised by Loan in order to properly retain the wafer during plasma or reactive ion etching procedures of La.

Regarding the gaps issue, La teaches that backside scrubbing removes micro defects, such as micro particles and hillocks and forms a flat plane backside surface (col.3, lines 59-64), thus eliminating gaps between the chucking surface and the backside of the wafer.

Regarding the limitation of claim 13, which is concerned with heat transfer system inside the chuck, such system is conventionally used in the processing of semiconductor devices, which is provided by Loan. Loan teaches the heat transfer system between the chuck and substrate, utilizing He gas (col.8, lines 10-16; col.21, lines 40-44). Therefore, one skilled in the art would have found it obvious to employ the heat transfer system of Loan in order to provide optimum thermal coupling between the wafer and the chuck while processing the wafer of La.

Regarding particular limitations of claims 16-18, which are concerned with specific order of performing steps, executed in a multiple cluster tool, which is equipped with load locks, aligner, transport module, processing module and cleaning module, first of all, it is noticed that cluster tools are widely employed in the art of semiconductor processing, because they allow to provide better control and increase the yield of fabrication process. Thus, Loan provides a multiple cluster tool, which is equipped with load locks, aligner, transport module, processing modules, etc. (Fig.4, 15; col.23, lines 1-35). Loan indicates that variety of other standardized components and modules for different processes can also be integrated in the cluster tool as desired (col.22, lines 67), thus providing a clear motivation to the skilled in the art to include any additional module in the cluster tool design, which is necessary for performing certain processing tasks. Because La teaches cleaning the backside of the wafer, utilizing a conventional equipment, and subsequent processing of the front side of the same wafer and Loan teaches a multiprocessing cluster tool in which variety of standardized components can be integrated, one skilled in the art would have found it obvious to integrate the cleaning equipment of La in the cluster tool of Loan in order to eliminate unnecessary exposure of processed wafers to environment and thus avoid additional contamination, provide better control of the fabrication process and improve its output.

Secondly, the sequence of steps in claims 16-18 is not specifically elucidated and selection of any order of performing steps is prima facie obvious in the absence of a new and unexpected results. Consult In re Burnhans, 154F.2d690, 69 USPQ 330 (CCPA 1946) and consult also Ex parte Rubin, 128 USPQ 440 (Bd.App.1959).

14. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over combined teaching of Prall and Guo and in view of Loan et al. (U.S. 6,136,725).

The teaching of Prall/Guo does not specifically provides for a heat transfer system inside the chuck. However, such system is conventionally used in the processing of semiconductor devices. Thus, Loan et al. (U.S. 6,136,725) provides the heat transfer system between the chuck and substrate, utilizing He gas. Therefore, one skilled in the art would have found it obvious to employ the system of Loan in the combined teaching of Prall and Guo in order to control the temperature and deposition environment around the wafer.

15. Therefore, combination of references renders claims 2, 3, 11-18 prima facie obvious and properly rejected under 35 U.S.C. 103(a).

16. References provided in PTO-892 show the general state of the art

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Kornakov whose telephone number is (703) 305-0400. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Randy Gulakowski can be reached on (703) 308-4333. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872 9310 for regular communications and (703) 872 9311 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308 2450.

Michael Kornakov
Examiner
Art Unit 1746

MK
July 30, 2002

RANDY GULAKOWSKI
SUPERVISORY PATENT EXAMINER
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